

PHP34NQ11T

N-channel TrenchMOS™ standard level FET

Rev. 01 — 17 May 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low on-state resistance
- Low thermal resistance.

1.3 Applications

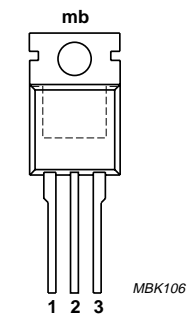
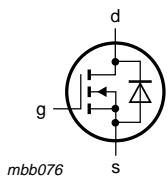
- DC-to-DC converters
- Switched-mode power supplies.

1.4 Quick reference data

- $V_{DS} \leq 110 \text{ V}$
- $I_D \leq 35 \text{ A}$
- $P_{tot} \leq 136 \text{ W}$
- $R_{DSon} \leq 40 \text{ m}\Omega$.

2. Pinning information

Table 1: Pinning - SOT78 (TO-220AB), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
mb	mounting base; connected to drain (d)		

SOT78 (TO-220AB)



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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PHP34NQ11T	TO-220AB	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads	SOT78

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

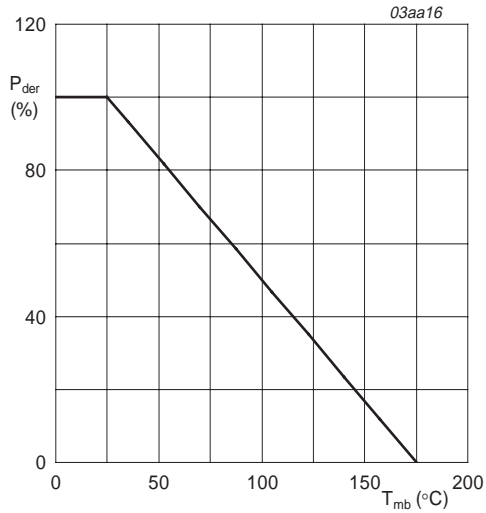
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	110	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	110	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	35	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	25	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	140	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	136	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C

Source-drain diode

I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	35	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	140	A

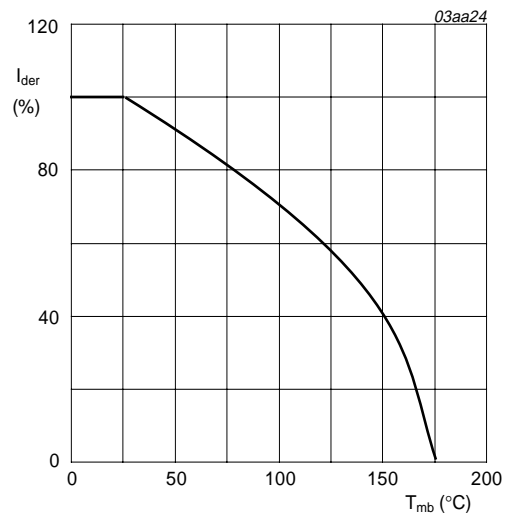
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 34\text{ A}$; $t_p = 0.05\text{ ms}$; $V_{DD} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ °C}$	-	115	mJ
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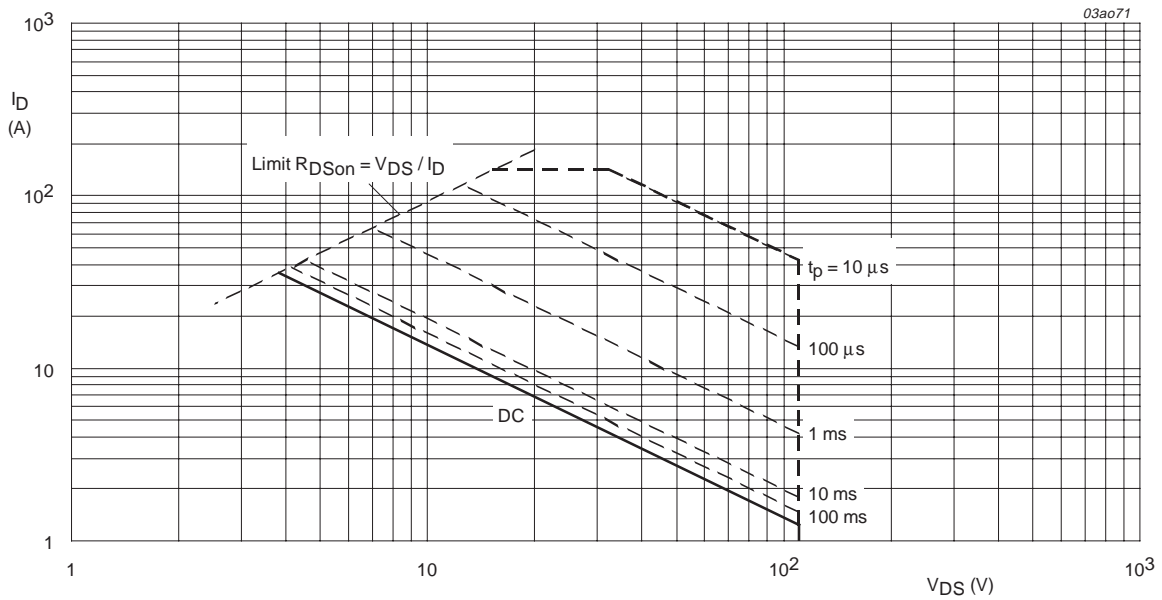
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 10 V$.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

5.1 Transient thermal impedance

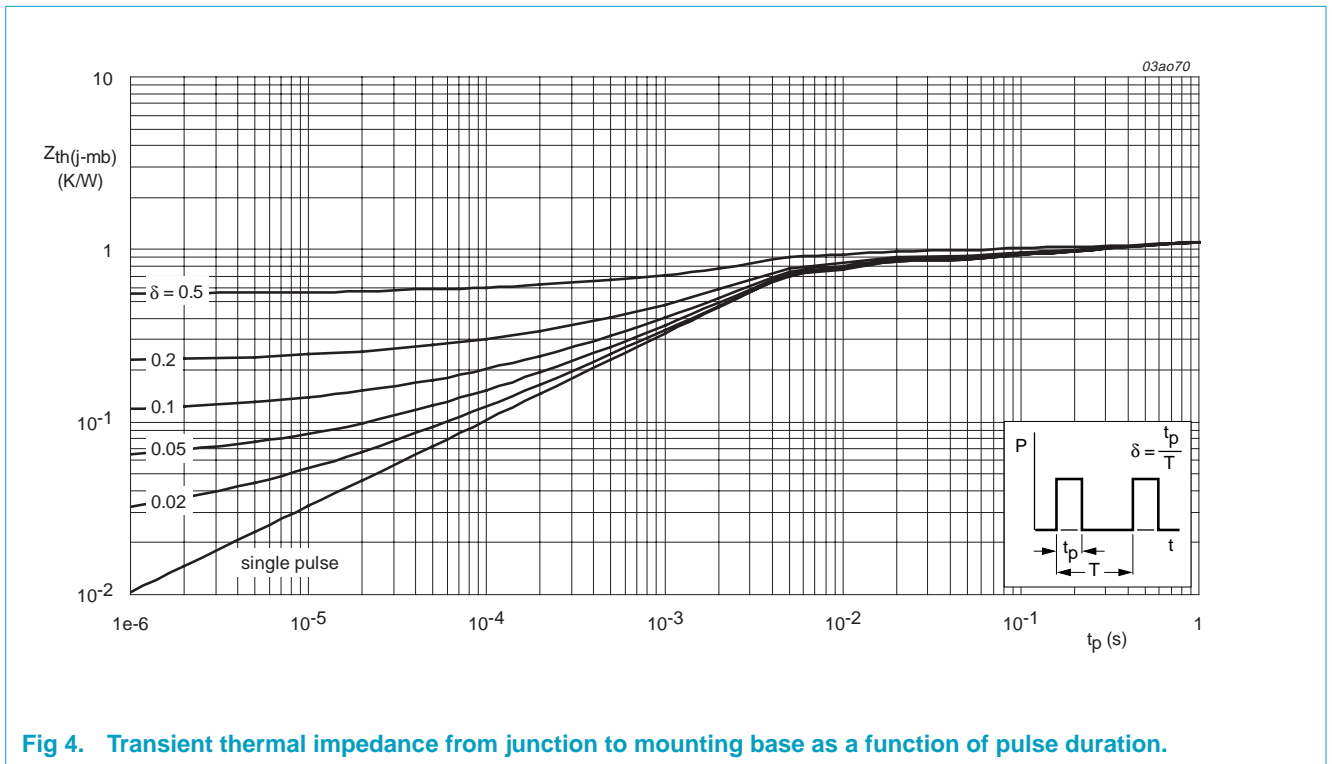
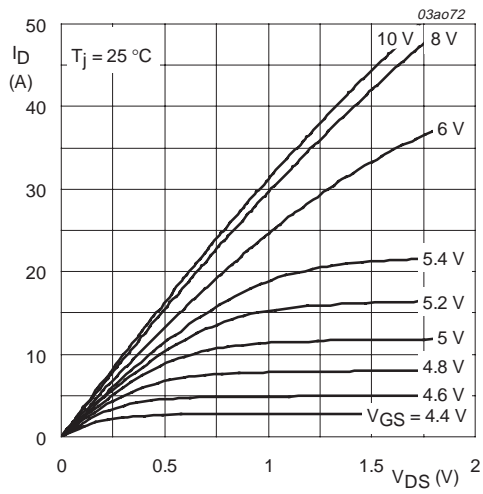


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

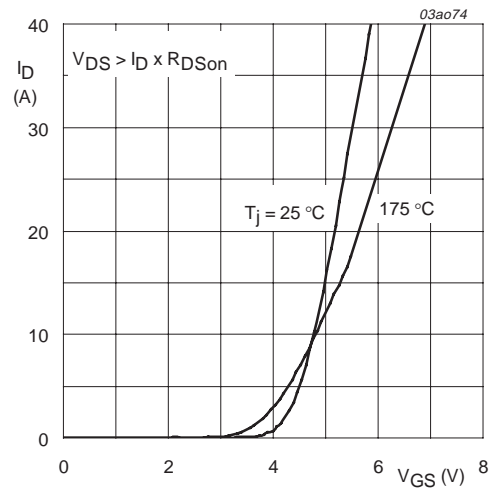
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V				
		T _j = 25 °C	110	-	-	V
		T _j = -55 °C	99	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 and 10				
		T _j = 25 °C	2	3	4	V
		T _j = 175 °C	1	-	-	V
		T _j = -55 °C	-	-	4.4	V
I _{DSS}	drain-source leakage current	V _{DS} = 100 V; V _{GS} = 0 V				
		T _j = 25 °C	-	-	10	μA
		T _j = 175 °C	-	-	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 17 A; Figure 7 and 8				
		T _j = 25 °C	-	35	40	mΩ
		T _j = 175 °C	-	-	108	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 34 A; V _{DD} = 80 V; V _{GS} = 10 V;	-	40	-	nC
Q _{gs}	gate-source charge	Figure 13	-	7	-	nC
Q _{gd}	gate-drain (Miller) charge		-	18	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	1700	-	pF
C _{oss}	output capacitance	Figure 11	-	230	-	pF
C _{rss}	reverse transfer capacitance		-	140	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 50 V; R _L = 1.5 Ω;	-	12	-	ns
t _r	rise time	V _{GS} = 10 V; R _G = 5.6 Ω	-	55	-	ns
t _{d(off)}	turn-off delay time		-	48	-	ns
t _f	fall time		-	38	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 17 A; V _{GS} = 0 V; Figure 12	-	0.85	1.5	V
t _{rr}	reverse recovery time	I _S = 17 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V	-	76	-	ns
Q _r	recovered charge		-	240	-	nC



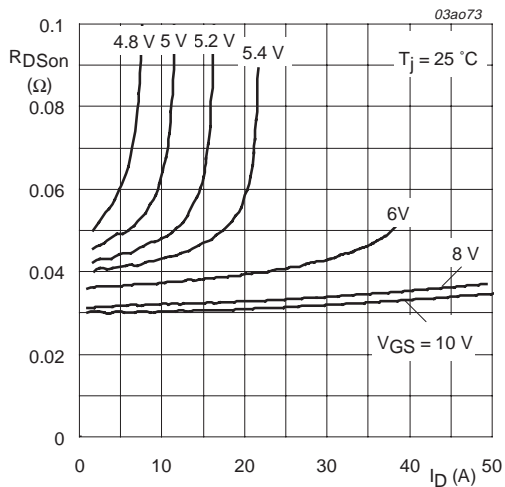
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



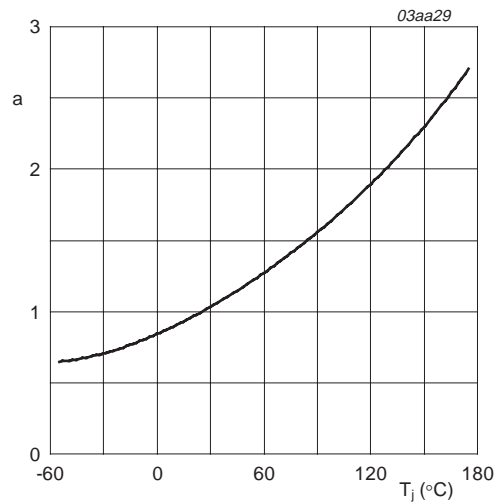
$T_j = 25\text{ °C}$ and 175 °C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



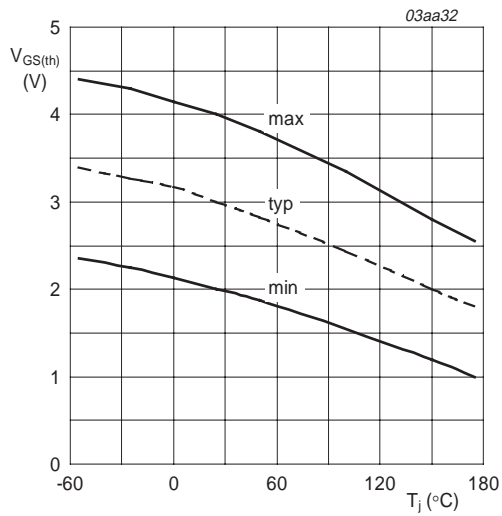
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



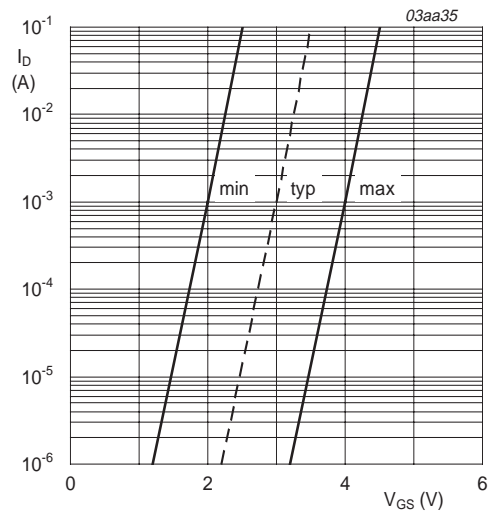
$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ °C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



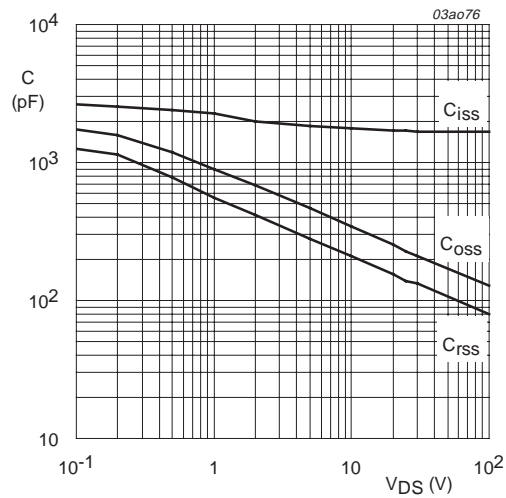
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



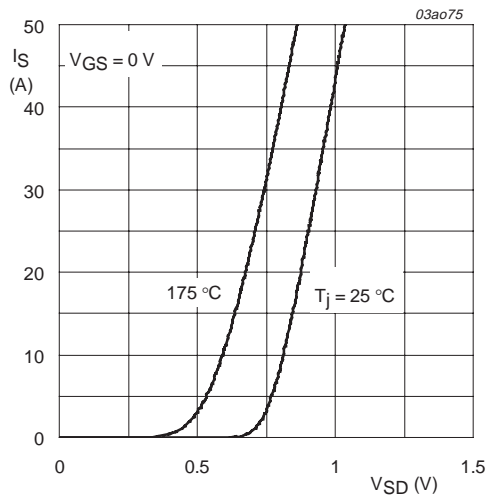
$T_J = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



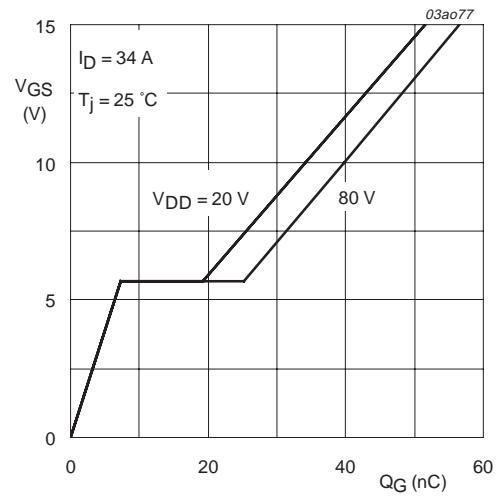
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$ and 175°C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 34\text{ A}$; $V_{DD} = 20\text{ V}$ and 80 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

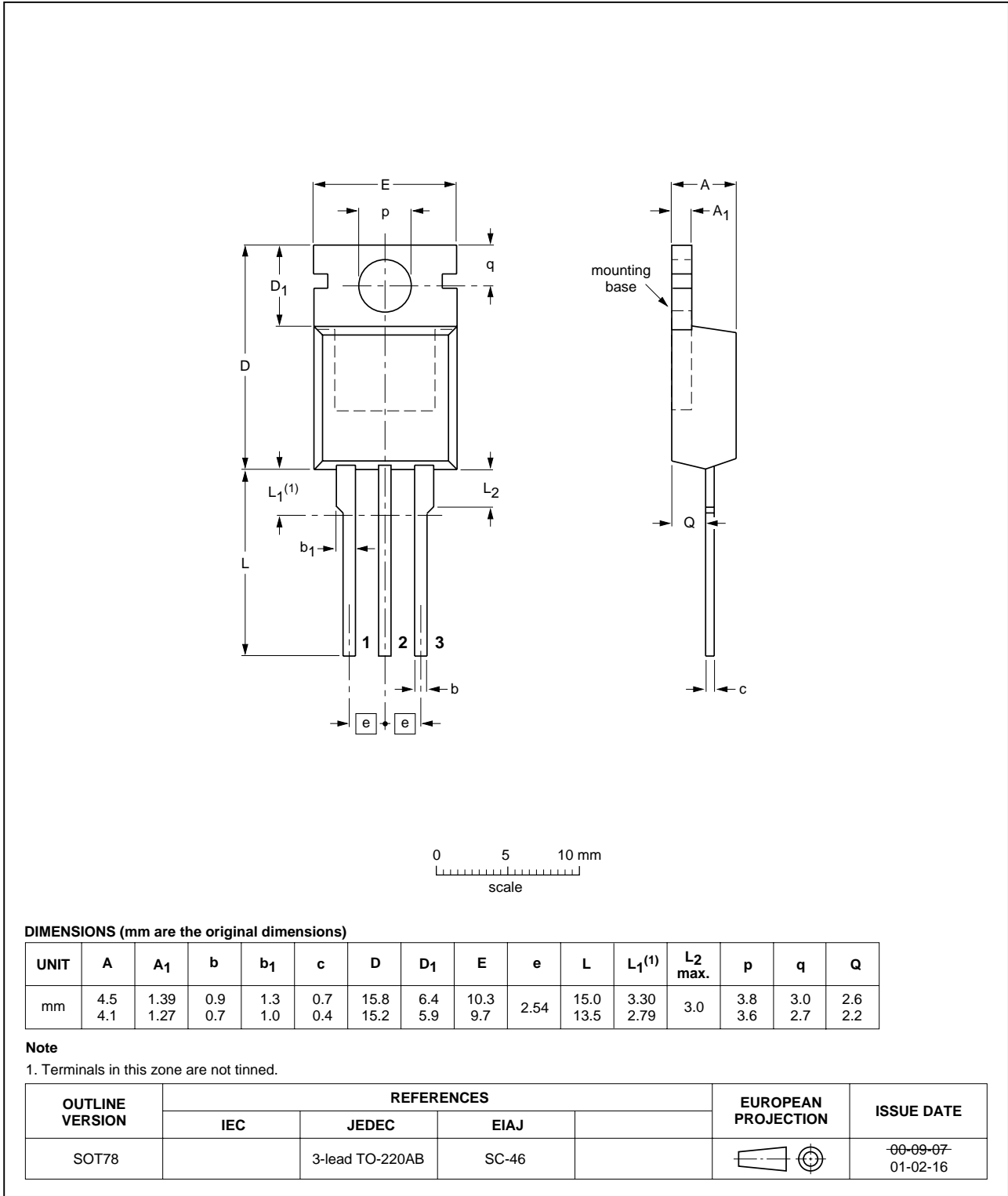


Fig 14. SOT78 (TO-220AB).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040517	-	Product data (9397 750 13184)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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